

6 storage means for holding a predetermined number N
7 of individual instructions, including at least one group of
8 M individual instructions to be executed in parallel, where
9 $M \leq N$, each individual instruction in the storage means
10 having associated therewith a pipeline identifier indicative
11 of the processing pipeline for executing that individual
12 instruction and a group identifier indicative of the group
13 of individual instructions to [be executed] which it is
14 assigned for execution in parallel;

15 group decoder means responsive to the group
16 identifier for causing all individual instructions having
17 the same group identifier to be executed [at the same time]
18 in parallel; and

19 pipeline decoder means responsive to the pipeline
20 identifier of the individual instructions in the group [to
21 supply] for causing each individual instruction in the group
22 [to be executed in parallel] to be supplied to an
23 appropriate processing pipeline.

1 2. (Amended) A computing system as in claim 1
2 wherein the storage means includes the at least one group of
3 individual instructions, and for each individual instruction
4 the storage means also includes the group identifier and the
5 pipeline identifier.

1 3. (Amended) A computing system as in claim 2
2 wherein each individual instruction in the at least one
3 group of individual instructions has associated therewith a
4 different pipeline identifier.

1 4. (Amended) A computing system as in claim 1
2 wherein the storage means holds [at least two groups of
3 instructions, and] a first group of individual instructions
4 to be executed in parallel and a second group of individual
5 instructions to be executed in parallel after the first

6 group, [all of] the individual instructions in each group
7 having associated therewith a common group identifier [are]
8 being placed adjacent to each other in the storage means.

1 5. (Amended) A computing system as in claim 4
2 wherein:

3 the storage means comprises a line in a cache
4 memory having a fixed number of storage locations;

5 the first group of individual instructions [to be
6 executed first] is placed at one end of the line in the
7 cache memory, and the second group of individual
8 instructions [in the group] to be executed [last] next is
9 placed [at the other end of the line in the cache memory]
10 next to the first group of individual instructions.

1 6. (Amended) A method of executing arbitrary
2 numbers of instructions in a stream of instructions in
3 parallel which have been compiled to determine which
4 instructions can be executed [at the same time,] in
5 parallel, the method comprising:

6 in response to the compilation, assigning a common
7 group identifier[s] to [sets] a group of instructions which
8 can be executed in parallel;

9 determining a processing pipeline for execution of
10 each instruction in [a] the group [to be executed;] of
11 instructions to be executed;

12 assigning a pipeline identifier to each
13 instruction in the group; and

14 placing a fixed number of the instructions in a
15 register, which number includes at least one group of
16 instructions having the common group identifier as well as
17 at least one other instruction having a different group
18 identifier [for execution by the pipelines].

1 7. (Amended) A method as in claim 6 further
2 comprising the step of executing [a] the group of
3 instructions in parallel.

1 8. (Amended) A method as in claim 7 wherein the
2 register holds at least two groups of instructions, and the
3 step of placing the instructions in the register for
4 execution by the processing pipelines comprises placing the
5 instructions in each group having associated therewith a
6 common group identifier adjacent to each other in the
7 register.

1 9. (Amended) A method as in claim 8 wherein the
2 step of executing a group of instructions in parallel
3 comprises coupling the register to detection means to
4 receive the group identifier of each instruction in the
5 register and the group identifier of the next group of
6 instructions to be supplied to the processing pipelines; and
7 supplying only the instructions with the next
8 group identifier to the processing pipelines. [execution
9 units.]

1 10. (Amended) In a computing system in which a
2 group[s] of individual instructions are executable in
3 parallel by processing pipelines, a method for supplying
4 each individual instruction in [a] the group to be executed
5 in parallel to [an] corresponding appropriate processing
6 pipelines, the method comprising:

7 storing in storage an instruction frame, the frame
8 including at least one group of individual instructions to
9 be executed in parallel, each individual instruction in the
10 group having associated therewith a pipeline identifier
11 indicative of the processing pipeline which will execute
12 that instruction and a group identifier indicative of the
13 group identification;

14 comparing the group identifier of each individual
15 instruction in the instruction frame [and a group] with an
16 execution identifier of those instructions to be next
17 executed [in parallel]; and

18 using the pipeline identifier of those individual
19 instructions to be next executed [in parallel to control an
20 execution unit] to execute [all] each of the individual
21 instructions in the group in separate processing pipelines.

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1 11. (Amended) In a computing system in which
2 groups of individual instructions are executable in parallel
3 by a set of processing pipelines, apparatus for routing each
4 instruction in a group to be executed in parallel to an
5 appropriate processing pipeline, the apparatus comprising:

6 storage for holding at least one group of
7 instructions to be executed in parallel, each instruction in
8 the group having associated therewith a pipeline identifier
9 indicative of the processing pipeline for executing that
10 instruction and a group identifier to designate among the
11 instructions present in the storage those instructions which
12 may be simultaneously supplied to the processing pipelines.

13 a crossbar switch having a first set of connectors
14 coupled to the storage for [receiving] transferring
15 instructions therefrom [and] to a second set of connectors
16 coupled to the processing pipelines;

17 [means] a router responsive to the pipeline
18 identifier of the individual instructions in the group for
19 routing individual instructions onto appropriate ones of the
20 second set of connectors, to thereby supply each instruction
21 in the group to be executed in parallel to the appropriate
22 processing pipeline.

1 12. Apparatus as in claim 11 wherein:

2 the first set of connectors [consists of] includes
3 a set of first communication buses, one for each instruction
4 in the storage;

5 the second set of connectors [consists of]
6 includes a set of second communication buses, one for each
7 processing pipeline; and

8 [the means] the router responsive to the pipeline
9 identifier comprises:

10 a set of decoders coupled to the storage,
11 each decoder to receive as a first input signal[s] the
12 pipeline identifier[s] of a corresponding instruction
13 in the storage and in response thereto supply as output
14 signals [a] corresponding switch control signals; and

15 a set of switches, coupled to the decoders to
16 receive the switch control signals, one switch at the
17 intersection of each of the first set of connectors
18 with each of the second set of connectors, the switches
19 providing connections in response to receiving the
20 corresponding switch control signal to thereby supply
21 each instruction in the group to be executed in
22 parallel to the appropriate processing pipeline.

1 13. (Amended) Apparatus as in claim 12 further
2 comprising:

3 detection means coupled to receive the group
4 identifier of each instruction in the storage and connected
5 to receive information regarding [the group identifier of]
6 the next group of instructions to be supplied to the
7 processing pipelines, and in response thereto supply a group
8 control signal; and

9 wherein the set of decoders coupled to the storage
10 are also coupled to the detection means to receive the group
11 control signal and in response thereto [supplies] supply a
12 switch control signal for only those instructions in the
13 group to be supplied to the processing pipelines.

1 14. (Amended) Apparatus as in claim 13 wherein
2 the detection means comprises a multiplexer coupled to
3 receive [each of] the group identifier[s] of each
4 instruction[s] in the storage and the group identifier of
5 the next group of instructions to be executed, and, in
6 response allow [compare them to the information regarding
7 the group identifier of] the next group of instructions to
8 be supplied to the processing pipelines.

1 15. (Amended) Apparatus as in claim 14 wherein
2 the multiplexer supplies an output signal to the decoders to
3 indicate the group identifier of the next group of
4 instructions to be supplied to the processing pipelines.

1 16. (Amended) In a computing system in which a
2 group[s] of individual instructions are executable in
3 parallel by processing pipelines, apparatus for routing each
4 instruction in a group to be executed in parallel to an
5 appropriate processing pipeline, the apparatus comprising:

6 a storage for holding an instruction frame, the
7 frame including at least one group of instructions to be
8 executed in parallel, each instruction in the group having
9 associated therewith a pipeline identifier indicative of the
10 processing pipeline to which that instruction is to be
11 issued and a group identifier indicative of the group
12 [identification];

13 a crossbar switch having a first set of connectors
14 coupled to the storage for receiving instructions therefrom
15 and a second set of connectors coupled to the processing
16 pipelines;

17 selection means connected to receive the group
18 identification of each instruction in the instruction frame
19 and connected to receive information about the group
20 identifier of those instructions to be next executed [in
21 parallel] for supplying in response thereto [an output

22 signal indicative of] a control signal to permit the next
23 [set] group of instructions to be executed in parallel; and
24 decoder means coupled to the selection means to
25 receive the [output] control signal and each of the pipeline
26 identifiers of the instructions in the storage for
27 selectively connecting ones of the first set of connectors
28 to ones of the second set of connectors to thereby supply
29 each instruction in the group to be executed in parallel to
30 the appropriate processing pipeline.

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1 17. (Amended) Apparatus as in claim 16 wherein
2 the first set of connectors consists of a set of first
3 communication buses, one for each instruction in the
4 storage;

5 the second set of connectors consists of a set of
6 second communication buses, one for each processing
7 pipeline;

8 the decoder means comprises a set of decoders
9 coupled to receive as first input signals the pipeline
10 identifiers and as second input signals information about
11 the group identifier of the next group of instructions to be
12 executed by the pipelines and in response thereto supply [as
13 output signals a] corresponding switch control signals; and

14 the crossbar switch includes a set of switches,
15 one at the intersection of each of the first set of
16 connectors with the second set of connectors, the switches
17 providing connections in response to receiving the switch
18 control signals to thereby supply each instruction in the
19 group to be executed in parallel to the appropriate
20 processing pipeline.

1 18. (Amended) Apparatus as in claim 17 wherein
2 the selection means coupled to the storage comprises a
3 multiplexer coupled to receive each of the group identifiers
4 of instructions in the storage, and [compare them] in

5 response to information regarding the group identifier of
6 the next group of instructions to be supplied to the
7 pipelines, enable appropriate instructions to be supplied to
8 the processing pipelines.

1 19. (Amended) Apparatus as in claim 18 wherein
2 the multiplexer supplies an output signal to the decoders to
3 select the group identifier of the next group of
4 instructions to be supplied to the processing pipelines.

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20. (Amended) In a computing system in which a
2 group[s] of individual instructions are executable in
3 parallel by processing pipelines, a method for transferring
4 each instruction in a group to be executed through a
5 crossbar switch having a first set of connectors coupled to
6 the storage for receiving instructions therefrom and a
7 second set of connectors coupled to the processing
8 pipelines, the method comprising:

9 storing in storage a set of instructions including
10 at least one group of instructions to be executed in
11 parallel, each instruction in the group having associated
12 therewith a unique pipeline identifier indicative of the
13 processing pipeline which will execute that instruction, and
14 also including at least one other instruction not in the at
15 least one group of instructions, which other instruction
16 also having associated therewith a pipeline identifier; and

17 using the pipeline identifiers of the individual
18 instructions in the at least one group of instructions which
19 are to be executed next to control switches between the
20 first set of connectors and the second set of connectors to
21 thereby supply each instruction in the group to be executed
22 in parallel to the appropriate processing pipeline.

1 21. A method as in claim 20 wherein the step of
2 using the pipeline identifiers comprises:

3 supplying the pipeline identifiers of the
4 individual instructions in the at least one group of
5 instructions to [a corresponding number of decoders,]
6 individual ones of a set of decoders, each of which provides
7 an output signal indicative of the pipeline identifiers of
8 the individual instruction supplied thereto; and

9 using the decoder output signals to control the
10 switches between the first set of connectors and the second
11 set of connectors to thereby supply each individual
12 instruction in the group to be executed in parallel to [the]
13 an appropriate processing pipeline.

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22. (Amended) A method as in claim 21 wherein
2 each of the individual instructions in the storage further
3 includes a group identifier to designate among the
4 instructions present in the storage which may be
5 simultaneously supplied to the processing pipelines, and the
6 method further comprises:

7 supplying information about the group identifier
8 of the next group of instructions to be executed by the
9 processing pipelines together with the group identifiers of
10 the individual instructions in the at least one group of
11 instructions to a selector;

12 comparing the group identifier of the next group
13 of instructions to be executed by the processing pipelines
14 with the group identifiers of the individual instructions in
15 the at least one group of instructions, to provide output
16 comparison signals; and

17 using both the output comparison signals and the
18 decoder output signals to control the switches [be
19 tween] between the first set of connectors and the second
20 set of connectors to thereby supply each instruction in the
21 group to be executed in parallel to the appropriate
22 processing pipeline.